IN THE SPECIFICATION:

Please amend paragraph number **[0006]** as follows:

[0006] Additional solutions have been developed in the prior art and are illustrated in United States Patent Nos. 5,585,675 ('675 patent) and 5,434,745 ('745 patent). The '675 patent discloses a packaging assembly for a plurality of semiconductor devices that provides for stacking of the semiconductor devices. The packaging assembly uses angularly offset ~~pad-to-pad~~ pad-to-pad via structures that are configured to allow three-dimensional stacking of the semiconductor devices. The electrical connection is provided to a via structure where multiple identical tubes are provided in which a semiconductor device is mounted and then one tube is mounted on top of another tube. The angularly offset via pads are provided through the stack tube structure for connection. One disadvantage with the angularly offset pad via structure is that the tubes must be precisely manufactured so that the vias are lined up properly. Further, the semiconductor devices must be set within strict tolerances for the tubes to stack one on top of another so the vias can be aligned properly as well.

Please amend paragraph number **[0007]** as follows:

[0007] The '745 patent discloses a stacked semiconductor device carrier assembly and a method for packaging interconnecting semiconductor devices. The carriers are constructed from a metal substrate onto which the semiconductor device attaches. Next, the semiconductor device is wired bonded to the conductor pattern on the substrate and each conductor is routed to the edge of the substrate where it is connected to a half circle ~~of~~ of a metallized through-hole. Again, the '745 patent discloses a ~~tube like~~ tube-like design with half circle vias for allowing interconnection to the stack of multiple semiconductor devices.

Please amend paragraph number **[0017]** as follows:

[0017] FIG. 7 is a cross-sectional view of a multiple semiconductor ~~devices~~ device (die) package that has a sealant about the interconnections;

Please amend paragraph number **[0020]** as follows:

[0020] FIG. 10 is a block diagram of an electronic system incorporating the semiconductor device of FIG. 2 and <u>the</u> present invention.

Please amend paragraph number **[0022]** as follows:

[0022] This protects the semiconductor devices 24 during the stacking and enables a variety of interconnections to be used between semiconductor devices 24, T-interposers 26, and/or substrates 22. The interconnection between semiconductor devices 24 or T-interposers 26 or substrates 22, or both, uses conductor traces, tape, wire bonding, conductive paste, or conductive adhesives, or any other type of suitable semiconductor interconnection technique known to one skilled in the art. The T-interposer 26 allows bond pads 28 of the semiconductor device 24 to be exposed, so no additional rerouting steps are required to reroute a bond pad 28 to the edges. This is advantageous over the prior art structures, such as the cubic design shown in drawing FIG. 1, in that the shell case or the interconnection requires additional processing in those materials and <u>additional</u> time. Further, the flanged edges forming the stem 27 of T-interposer 26 allow direct connection to the bond pads 28 and contact to all four sides of semiconductor devices 24. This allows increased interconnect density between a substrate and a plurality of semiconductor devices.

Please amend paragraph number **[0024]** as follows:

[0024] Referring to drawing FIG. 3, further illustrated is an inverted T-interposer 26 as shown in drawing FIG. 2. Again, T-interposer 26 can be manufactured to match the same CTE of the semiconductor device 24 or the semiconductor device substrate 22 used for each of semiconductor devices 24, or both. This allows T-interposer 26 to serve as a thermal or heat dissipation device between each semiconductor device 24 while allowing for greater heat dissipation than would otherwise be possible were the semiconductor devices 24 stacked directly upon each other. Further, T-interposer 26 provides electrical insulation between each semiconductor device 24 that would not be otherwise possible were the semiconductor devices to

be stacked one upon another such as in the prior art described in drawing FIG. 1. Additionally, the T-interposer 26 may be comprised of two different materials to provide both thermal conductivity from one semiconductor device and thermal insulation with respect to a second semiconductor device. For instance, the stem 27 may be of a thermally conductive material while the T-bar members 29 are formed of a thermally insulative material, the stem 27 may be joined to the T-bar member(s) 29 by any suitable means, such as adhesive bonding, etc. The ~~T-interposer~~ T-interposer 26 of the present invention provides for much greater bonding edge relief for different types of connection devices with respect to the bond pad location on the active surface of the semiconductor device 24 than that shown in the prior art device illustrated in drawing FIG. 1 and greater insulation capacity for the bond pads 28 of the semiconductor devices 24 with the ~~T-interposer~~ T-interposer 26 in place. Finally, a top T-interposer 26 is further provided for capping the device to protect and promote heat transfer from the last semiconductor device 24 forming the multiple stacked unit 20.

Please amend paragraph number **[0026]** as follows:

[0026] Referring to drawing FIG. 4, illustrated is a cross-section diagram of multiple semiconductor devices 38 and 40 being mounted to a single T-interposer 26. T-interposer 26 is mounted to a substrate 36. Substrate 36 includes ~~bonding~~ bond pads/circuits 28 thereon. Semiconductor device 38 can be a processor type semiconductor device while semiconductor device 40 can be a memory type semiconductor device. Semiconductor device 38 and semiconductor device 40 are interconnected via bond pads 28 and further connected to bond pads or circuits 28 on substrate 36. Additionally, the bonding wire from one bond pad or circuit 28, such as on ~~die~~ device 40, can connect directly to the device structure to which the substrate 36 is to be permanently mounted. This can be the actual circuit board, such as a mother board used in a computer system. Of course, other direct connection options will be readily apparent to one skilled in the art.

Please amend paragraph number **[0028]** as follows:

[0028] Referring to drawing FIG. 6, depicted is an alternative embodiment T-interposer 126 of the present invention, which is similar to the embodiment of the T-interposer 26 illustrated in drawing FIG. 3. As illustrated in drawing FIG. 6, the T-interposer 126 includes additional recessed sections all around. The entire recessed periphery allows semiconductor devices that have connection pads around the entire perimeter of the device to be exposed for connection. In this manner, greater inter-connectivity is achieved with the ability to connect very dense interconnected circuit devices to other semiconductor devices. Additionally, ball weld spots 128 are provided as well and allow direct electrical and mechanical connection of any subsequent semiconductor devices. The stem 127 of the ~~T-interposer~~ T-interposer 126 includes T-members 129 therearound and substantially horizontal surface 129′ located thereabove as described hereinbefore with respect to T-interposer 26.

Please amend paragraph number **[0029]** as follows:

[0029] Referring to drawing FIG. 7, illustrated is a cross-sectional view of a multiple stack unit 20 that is completely sealed or packaged. Again, a substrate 22 is provided upon which a first semiconductor device 24 is mounted ~~with an~~ with a T-interposer 26 mounted to the first semiconductor device 24. A final cap or top T-interposer 26 is further provided on top of the entire stack unit 20. Lastly, an epoxy interconnect 50 is provided for sealing and/or packaging and electrically isolating the bonding performed between the multiple semiconductor devices 24. If desired, the top of the unit 20 may include a heat sink 52 of suitable type material which may include one or more fins 54 (shown in dashed lines) for additional thermal control of the heat from the unit 20.

Please amend paragraph number **[0030]** as follows:

[0030] Referring to drawing FIG. 8, illustrated is another embodiment of the ~~T-interposer~~ T-interposer 26 of the present invention in a stacked arrangement between semiconductor devices 40 which are electrically connected by wires 56 to circuits 58 of the

substrate 36. In this embodiment of the T-interposer 26 of the present invention, one T-bar member 29 has a greater length or extends farther than the opposing T-bar member 29 of the T-interposer 26 to provide greater bonding edge relief for different types of connection devices with respect to the bond pad location on the active surface of the semiconductor device 24 than the bonding edge relief provided by the T-bar member 29 on the other side of the T-interposer 26. In this manner, the ~~T-interposer~~ T-interposer 26 is not centrally located on a portion of the active surface of the semiconductor device 40 but, rather, is located off-center on a portion of the active surface of the semiconductor device 40. Such a T-interposer 26 allows for the accommodation of differing sizes and shapes of semiconductor devices 40 and bond pad arrangements thereon for interconnection to the circuits 58 of substrate 36.

Please amend paragraph number **[0031]** as follows:

[0031] Referring to drawing FIG. 9, illustrated is another embodiment of the T-interposer 26 of the present invention where the T-interposer 26 includes a plurality of stems 27 and T-bar members 29 to form the same, each stem 27 located on a portion of the active surface of a semiconductor device 40 which is, in turn, located on a substrate 36 having circuits 58 located thereon connected by wires 56 while wires 62 electrically connect the semiconductor devices 40 located on surface 29′ of the T-interposer 26 to the circuits 60 located thereon. In this manner, the T-interposer 26 helps to increase the density of the semiconductor devices 40 located on the substrate 36 while providing thermal control of the heat generated from the semiconductor devices 40 located on the substrate 36 and on the surface 29′ of the T-interposer 26.

Please amend paragraph number **[0033]** as follows:

[0033] The use of the T-interposer 26 for stacking bare dies has several advantages over prior art solutions. One advantage is that it reduces stack stresses or bending. Further, the T-interposer allows easier reworking of any bond interconnect when necessary. Additionally, as there ~~is no~~ are no stress problems inherit in stacking semiconductor devices upon other devices

as any number of devices can be stacked with T-interposer 26 used in separating device from device, thus allowing for greater device densities for memory devices and other type semiconductor devices. Also, several types of interconnect methods are possible with the T-interposer, such as wire bonding, ball bonding, flip chip bonding, etc. Additional advantages include the bond pads of each semiconductor device being protected from one another in the device stack. Thermal and mechanical properties are improved because of the use of the T-interposer. The improved thermal and mechanical properties also allow for increased semiconductor device density for memory chips and SIMM type devices.

Please amend paragraph number **[0035]** as follows:

[0035] As shown in drawing FIG. 10, an electronic system 130 includes an input device 132 and an output device 134 coupled to a processor device 136 which, in turn, is coupled to a memory device 138 incorporating the exemplary ~~integrated circuit die~~ <u>semiconductor device</u> 24 and T-interposer 26 of drawing FIG. 2.